CLAIMS

What is claimed is:

1. An integrated circuit comprising:

clock generation circuitry to generate a master clock signal and at least one other clock signal transmitted through a clock distribution tree to a circuit component, the circuit component receiving the master clock signal at a first component block; and

bypass logic to define a bypass path to allow a second component block of the circuit component to receive the master clock signal, wherein the first and second components are controlled by a common clock domain in response to the master clock signal.

2. The integrated circuit of claim 1, wherein the bypass logic includes a switch that allows for the coupling of either the master clock signal or the other clock signal to the second component block of the circuit component.

3. The integrated circuit of claim 2, wherein the switch is responsive to a master select signal to select the master clock signal for coupling to the second component block of the circuit component.

4. The integrated circuit of claim 1, wherein the bypass logic includes a bypass switch located in the second component block of the circuit component.

5. The integrated circuit of claim 4, wherein the bypass switch is responsive to a bypass activation signal to activate the bypass path.

6. The integrated circuit of claim 1, further comprising a default path to allow the second component block of the circuit component to receive the other clock signal such that the clock domain of the second component block of the circuit component is different from the clock domain of the first component block of the circuit component.

7. The integrated circuit of claim 6, wherein the default path is automatically selected when the integrated circuit powers up.

8. The integrated circuit of claim 7, wherein the bypass path is selected by a user.

9. The integrated circuit of claim 8, wherein selecting the bypass path further includes utilizing software to write a bit to a clocking register to instruct the circuit component to use the bypass path.

10. A method comprising:

designing a plurality of circuit components on an integrated circuit that achieve a clock skew less than a predetermined minimum;

designing a clock distribution tree for the plurality of circuit components on the integrated circuit to achieve the clock skew across all combinable circuit components and component blocks of the circuit components; and

for at least one of the plurality of circuit components,

defining two signal paths:

a default path; and

a bypass path.

11. The method of claim 10, wherein the at least one circuit component includes a first component block and a second component block, further comprising:

clocking the first component with a master clock signal; and

clocking the second component block with a circuit component clock signal.

12. The method of claim 11, wherein the bypass path allows the second component block to receive the master clock signal such that a clock domain of the second component block of the at least one circuit component is the same as a clock domain of the first component block of the at least one circuit component.

13. The method of claim 12, wherein the bypass path includes bypass logic having a bypass switch located in the second component block of the at least one circuit component.

14. The method of claim 13, wherein the bypass switch is responsive to a bypass activation signal to activate the bypass path.

15. The method of claim 11, wherein the default path allows the second component block of the at least one circuit component to receive the circuit component clock signal such that the clock domain of the second component block of the circuit component is different from the clock domain of the first component block of the circuit component.

16. The method of claim 15, wherein the default path is automatically selected when the integrated circuit powers up.

17. The method of claim 11, further comprising determining if the integrated circuit is functional, if not,

selecting the bypass path.

18. The method of claim 17, wherein selecting the bypass path further includes utilizing software to write a bit to a clocking register to instruct the at least one circuit component to use the bypass path.

19. The method of claim 11, wherein the bypass path is selected by a user.

20. A system comprising:

a processor coupled to memory; and

an integrated circuit coupled to the processor, the integrated circuit including:

clock generation circuitry to generate a master clock signal and at least one other clock signal transmitted through a clock distribution tree to a circuit component, the circuit component receiving the master clock signal at a first component block; and

bypass logic to define a bypass path to allow a second component block of the circuit component to receive the master clock signal, wherein the first and second components are controlled by a common clock domain in response to the master clock signal.

21. The system of claim 20, wherein the bypass logic includes a switch that allows for the coupling of either the master clock signal or the other clock signal to the second component block of the circuit component.

22. The system of claim 21, wherein the switch is responsive to a master select signal to select the master clock signal for coupling to the second component block of the circuit component.

23. The system of claim 20, wherein the bypass logic includes a bypass switch located in the second component block of the circuit component.

24. The system of claim 23, wherein the bypass switch is responsive to a bypass activation signal to activate the bypass path.

25. The system of claim 20, further comprising a default path to allow the second component block of the circuit component to receive the other clock signal such that the clock domain of the second component block of the circuit component is different from the clock domain of the first component block of the circuit component.

26. The system of claim 25, wherein the default path is automatically selected when the integrated circuit powers up.

27. The system of claim 26, wherein the bypass path is selected by a user.

28. The system of claim 27, wherein selecting the bypass path further includes, the processor utilizing software stored in memory to write a bit to a clocking register to instruct the circuit component to use the bypass path.